



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
| 10/021,374      | 10/30/2001  | Gayvin E. Stong      | 10010660-1          | 2639             |

7590 06/22/2004

AGILENT TECHNOLOGIES, INC.  
Legal Department, DL429  
Intellectual Property Administration  
P.O. Box 7599  
Loveland, CO 80537-0599

EXAMINER

KERVEROS, JAMES C

ART UNIT

PAPER NUMBER

2133

DATE MAILED: 06/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/021,374

Applicant(s)

STONG ET AL

Examiner

James C Kerveros

Art Unit

2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 26 February 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-25 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 October 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 4.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

**DETAILED ACTION**

1. Claims 1-25 are pending and are hereby presented for examination.

***Drawings***

2. The drawings are objected to because in FIGS. 1, 2 and 3, functional blocks (104, 107, 108), (210-217) and (301-304) require descriptive legends. Suitable descriptive legends may be used subject to approval by the Office, or may be required by the examiner where necessary for understanding of the drawing. They should contain as few words as possible.
3. Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Lepejian et al. (US 5974579), ISSUED: October 26, 1999.

Regarding independent Claims 1, 7 and 13, Lepejian discloses an apparatus and method (FIGS. 1, 5 and 6), comprising:

A memory element (memory array 90) having one or more impermissible operations, such as memory faults occurring during read / write operations, a plurality of memory access lines located between de-skewing circuit 70 and memory array 90, in FIG. 1.

A code generator (Encoded Data Generator 50 coupled to the Pattern Counter 22 in the controller 10, FIG. 6) and generating a test code (encoded data 12) in response to a clock signal, a decoder (data decoder 85) accepting the test code (12) and generating at least two output lines (86) which decodes the encoded data 12.

When in a decode enabled condition (Test Mode On via Mode Control), the output lines (86) are responsive to the test code (encoded data 12) and reflect a value on the output lines (86) that when combined with respective memory access lines located between de-skewing circuit 70 and memory array 90, FIG. 1, the test mode

Art Unit: 2133

disables the impermissible operations such as the memory faults occurring during read / write operations. During the impermissible operations, address filter 50 responds to the pseudo-random sequence of addresses so as to lock out only those illegal addresses from the smaller address space, by generating an "ADRR HALT" signal 52 when the address space of the second (smaller) memory 91 has been exceeded, FIG. 1.

When the decoder (data decoder 85) is in a decode disabled condition (Test Mode "Off" via Mode Control) such as during the operational mode, the output lines (86) reflect a value that when combined with the respective memory access lines located between de-skewing circuit 70 and memory array 90, FIG. 1, the test mode enables all possible Read /Write memory operations.

Regarding independent Claim 20, Lepejian discloses a method for built in self test (BIST) of a printed circuit board (PCB) including multiple IC circuit (100, 100-1...) with memory elements, FIG. 1, comprising:

Storing known seed values (test patterns) into a plurality of registers in the finite state machine BIST on the printed circuit board, (not shown) FIG. 1, and placing the printed circuit board (PCB) in a test code enable condition, such as (Test Mode On via Mode Control), using standard JTAG / BIST, which enable BIST and disable the normal operation of the circuit and storing the seed values from the finite state machine BIST into test code generator (Encoded Data Generator 50, FIG. 6).

Stimulating the printed circuit board with a clock signal, (address clock 13), in FIG. 1.

Art Unit: 2133

Generating a test code test code (12) for corresponding to (Encoded Data Generator 50, FIG. 6) in response to a clock signal (address clock 13).

Mapping each generated test code using decoder (data decoder 85) for accepting the test code (12) and generating at least two output lines (86), which decodes the encoded data 12.

When in a decode enabled condition (Test Mode On via Mode Control), the output lines (86) are responsive to the test code (encoded data 12) and reflect a value on the output lines (86) that when combined with respective memory access lines located between de-skewing circuit 70 and memory array 90, FIG. 1, the test mode disables the impermissible operations such as the memory faults occurring during read / write operations. During the impermissible operations, address filter 50 responds to the pseudo-random sequence of addresses so as to lock out only those illegal addresses from the smaller address space, by generating an "ADRR HALT" signal 52 when the address space of the second (smaller) memory 91 has been exceeded, FIG. 1.

When the decoder (data decoder 85) is in a decode disabled condition (Test Mode "Off" via Mode Control) such as during the operational mode, the output lines (86) reflect a value that when combined with the respective memory access lines located between de-skewing circuit 70 and memory array 90, FIG. 1, the test mode enables all possible Read /Write memory operations.

Comparing a resulting test signature (output data 82) with a known good test signature (input data 81) using data comparator (80) which compares the output data 82

Art Unit: 2133

from embedded memory 90 with the corresponding input data 81 and reports the results in a pass/fail format on test output line 19.

Regarding Claims 2, 3, 8, 9, 14, 15, 21 and 22, Lepejian discloses a code generator comprising a counter (see Pattern Counter 22, FIG. 6), and a pseudo-random generator, such as address generator (40, FIG. 20) based on a clocked shift register with linear feedback defined by a primitive polynomial.

Regarding Claims 4 and 16, Lepejian discloses a memory element (memory array 90) comprising a multiple port memory element, having control signal 83, address signals 84 and data signals 81 coupled to the embedded memory under test.

Regarding Claims 5, 6, 10-12, 17, 18 and 23-25, Lepejian discloses (data decoder 85) in a decode enabled condition, such as (Test Mode On via Mode Control), which maps each test code value (encoded data 12) to a unique state such logic level "1" or "0" at the output lines (86) and maps more than one test code value (encoded data 12).

Regarding Claim 19, Lepejian discloses test code generators, which receive the same clock signal (address clock 13), FIG. 1.

### ***Conclusion***

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

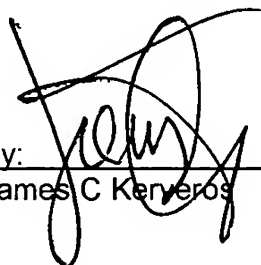
Art Unit: 2133

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

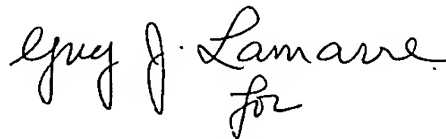
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE  
Examiner's Fax: (703) 746-4461  
Email: [james.kerveros@uspto.gov](mailto:james.kerveros@uspto.gov)

Date: 15 June 2004  
Office Action: Non-Final Rejection

By:   
James C Kerveros

Examiner  
Art Unit 2133

  
for

Albert DeCady  
Primary Examiner